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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,513	01/14/2002	Jimmie Earl DeWitt JR.	AUS920010715US1	2909

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EXAMINER	
LOHN, JOSHUA A	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,513	DEWITT ET AL.	
	Examiner	Art Unit	
	Joshua A Lohn	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8-13,15,16,18-23,25,26 and 28-30* is/are rejected.

7)☒ Claim(s) *4,7,14,17,24 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 6, 8-13, 15, 16, 18-23, 25, 26, and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Dockser, United States Patent number 6,006,030, published December 21, 1999.

As per claim 1, Dockser discloses a method for processing an instruction within a processor, wherein the processor processes a plurality of types of interruptions, and wherein the processor comprises a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are active within the processor (Dockser, col. 4, lines 23-32), the method comprising: executing an instruction within the processor (Dockser, col. 4, lines 26-27); receiving an interruption signal by the processor (Dockser, col. 5, lines 46-47, where the detector interrupts the processing when detecting exception events); in response to receiving the interruption signal, determining whether a trap mode is to remain active during interruption processing (Dockser, col. 5, lines 47-55); in response to a determination that the trap mode is to be deactivated during interruption processing, deactivating the trap mode (Dockser, col. 6, lines 30-32, where the exception processing is an interrupt of the application, col. 6, lines 33-34); and invoking an interruption handler to perform in interruption processing for the received interruption signal (Dockser, col. 6, lines 17-32).

As per claim 2, Dockser discloses indicating whether the trap mode is active or inactive using a trap mode field within the processor (Dockser, col. 5, lines 50-55).

As per claim 3, Dockser discloses wherein a first trap mode field indicates that a single-step trap mode is active (Dockser, col. 5, lines 46-55, where single-step mode is always active when trapping is active, because the detector receives all instructions in an effort to detect exceptions).

As per claim 5, Dockser discloses indicating whether a trap mode is to remain active during interruption processing using a trap mode conditioning field within the processor (Dockser, col. 5, lines 50-55).

As per claim 6, Dockser discloses a first trap mode conditioning field conditions activity of a single-step trap mode (Dockser, col. 5, lines 46-55, where single-step mode is always active when trapping is active, because the detector receives all instructions in an effort to detect exceptions).

As per claim 8, Dockser discloses performing a trace operation prior to deactivating the trap mode (Dockser, col. 5, lines 46-55, where the detection acts as a trace operation on all instructions prior to trapping).

As per claim 9, Dockser discloses reactivating the trap mode after interruption processing (Dockser, col. 6, lines 30-32, where the trap mode is only temporarily deactivated during processing).

As per claim 10, Dockser discloses performing a trace operation after reactivating the trap mode (Dockser, col. 5, lines 46-55, where reactivating the detector resumes the monitoring of all instructions, acting as a trace).

As per claim 11, Dockser discloses a processor that performs operations specified by instructions fetched from a memory, the processor comprising: means for maintaining a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are present within the processor (Dockser, col. 4, lines 23-32); means for fetching instructions from memory; means for executing an instruction within the processor (Dockser, col. 4, lines 23-44); means for receiving a plurality of types of interruptions (Dockser, col. 5, lines 20-30, where the list includes a plurality o types of exceptions, which act as interrupts on the application, col. 6, lines 33-34); means for determining whether a trap mode is to remain active during interruption processing in response to receiving an interruption (Dockser, col. 5, lines 47-55); means for deactivating a trap mode in response to a determination that the trap mode is to be deactivated during interruption processing (Dockser, col. 6, liens 30-32); and means for invoking an interruption handler to perform interruption processing for a received interruption (Dockser, col. 6, line 17-32).

As per claim 12, Dockser discloses means for maintaining a trap mode field within the processor to indicate whether the trap mode is active or inactive (Dockser, col. 5, lines 50-55).

As per claim 13, Dockser discloses a first trap mode field indicates that a single-step trap mode is active (Dockser, col. 5, lines 46-55, where single-step mode is always active when trapping is active, because the detector receives all instructions in an effort to detect exceptions).

As per claim 15, Dockser discloses means for maintaining a trap mode conditioning field within the processor to indicate whether a trap mode is to remain active during interruption processing (Dockser, col. 5, lines 50-55).

As per claim 16, Dockser discloses a first trap mode conditioning field conditions activity of a single-step trap mode (Dockser, col. 5, lines 46-55, where single-step mode is always active when trapping is active, because the detector receives all instructions in an effort to detect exceptions).

As per claim 18, Dockser discloses means for performing a trace operation prior to deactivating the trap mode (Dockser, col. 5, lines 46-55, where the detection acts as a trace operation on all instructions prior to trapping).

As per claim 19, Dockser discloses means for reactivating the trap mode after interruption processing (Dockser, col. 6, lines 30-32, where the trap mode is only temporarily deactivated during processing).

As per claim 20, Dockser discloses means for performing a trace operation after reactivating the trap mode (Dockser, col. 5, lines 46-55, where reactivating the detector resumes the monitoring of all instructions, acting as a trace).

As per claim 21, Dockser discloses a computer program product in a computer-readable medium for use in a data processing system for processing an instruction within a processor (Dockser, col. 4, lines 33-36), wherein the processor processes a plurality of types of interruptions, and wherein the processor comprises a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are active within the processor (Dockser, col. 4, lines 23-32), the computer program product comprising: means for executing an instruction within the processor (Dockser, col. 4, lines 26-27); means for receiving an interruption signal by the processor (Dockser, col. 5, lines 46-47, where the detector interrupts the process when

detecting exception events); means for determining whether a trap mode is to remain active during interruption processing in response to receiving the interruption signal (Dockser, col. 5, lines 47-55); means for deactivating the trap mode in response to a determination that the trap mode is to be deactivated during interruption processing (Dockser, col. 6, lines 30-32, where the exception processing is an interrupt of the application, col. 6, lines 33-34); and means for invoking an interruption handler to perform interruption processing for the received interruption signal (Dockser, col. 6, lines 17-32).

As per claim 22, Dockser discloses means for indicating whether the trap mode is active or inactive using a trap mode field within the processor (Dockser, col. 5, lines 50-55).

As per claim 23, Dockser discloses a first trap mode field indicates that a single-step trap mode is active (Dockser, col. 5, lines 46-55, where single-step mode is always active when trapping is active, because the detector receives all instructions in an effort to detect exceptions).

As per claim 25, Dockser discloses means for indicating whether a trap mode is to remain active during interruption processing using a trap mode conditioning field within the processor (Dockser, col. 5, lines 50-55).

As per claim 26, Dockser discloses a first trap mode conditioning field conditions activity of a single-step trap mode (Dockser, col. 5, lines 46-55, where single-step mode is always active when trapping is active, because the detector receives all instructions in an effort to detect exceptions).

As per claim 28, Dockser discloses means for performing a trace operation prior to deactivating the trap mode (Dockser, col. 5, lines 46-55, where the detection acts as a trace operation on all instructions prior to trapping).

As per claim 29, Dockser discloses means for reactivating the trap mode after interruption processing (Dockser, col. 6, lines 30-32, where the trap mode is only temporarily deactivated during processing).

As per claim 30, Dockser discloses means for performing a trace operation after reactivating the trap mode (Dockser, col. 5, lines 46-55, where reactivating the detector resumes the monitoring of all instructions, acting as a trace).

Allowable Subject Matter

Claims 4, 7, 14, 17, 24, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on included form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (571) 272-3661. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAL

SCOTT BADERMAN
PRIMARY EXAMINER